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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED

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Technology Center 2100

Application Number: 10/679,725
Filing Date: October 06, 2003
Appellant(s): FISCHER ET AL.

Craig J. Cox
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 29, 2007 appealing from the Office action mailed August 21, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-3, 9-11 and 15-17.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

GROUNDS OF REJECTION NOT ON REVIEW

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief. Whether claims 3, 11 and 17 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou et al., U. S. Patent 6,047,248.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

7,076,679	Fischer et al.	July 11, 2006
6,047,248	Georgiou et al.	April 4, 2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

Claims 1, 10 and 15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 8 and 15 of U.S. Patent 7,076,679. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention comprising a CPU having multiple clock zones where each clock zone includes at least one sensor, a variable frequency clock generator and a controller for controlling the operating frequency of the variable frequency clock generator. The claims of the patent are directed to a species of the genus recited in the claims 1, 10 and 15 of application 10/679,725. The claims of application 10/679,725 recite a generic controller that would have been obvious in view of the first and second controllers recited in claims 1, 8 and 15 of the patent because it would have been obvious to one of ordinary skill in the art that the frequency adjustment communications with the other clock zones recited in the patent claims could have been communicated in a generic manner using the generic controller recited in application claims 1, 10 and 15.

Claim Rejections - 35 USC § 103

Claims 1-3, 9-11 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou et al., U. S. Patent 6,047,248.

Per claims 1, 2, 9, 10, 15 and 16:

A) Georgiou et al teach the following claimed items:

1. a CPU (figure 1) having multiple clock zones with the multiple functional units 116-1 through 116-k and their associated control circuitry in elements 130, 330 and 430 of figure 1 and at column 5, lines 1-8 (each functional unit is independently controllable as to its clock frequency);

2. at least one sensor/temperature sensor (T1 – Tk) that generates a power signal (125) indicative of a power supply voltage (on-chip voltage regulator 330, VDD 325) within the clock zone (116-1 through 116-k) with temperature sensors T1 through Tk in figure 1, with figure 5b, at column 3, lines 31-40 and at column 4, lines 18-46;

3. a variable frequency clock generator with the clock input circuitry of each functional unit associated with clock input 425 of figure 1, with the associated functional units clock circuitry in figure 4 and at column 8, lines 37-67;

4. a controller for controlling an operating frequency of the clock generator in response to the power signal (125) with temperature decoder 130 of figure 1, with decoder selector 460, MUX select and the associated multiplexer 470 of figure 4, at column 4, lines 27-51 and at column 8, lines 50-67.

B) The claims differ from Georgiou et al in that Georgiou et al fails to explicitly teach the controller controlling an operating frequency of the clock generator in response to communications from other clock zones as claimed.

C) However, Georgiou describes that synchronization problems may occur when clock frequencies are varied to different portions of a chip and there is a need for controlling power dissipation of a synchronous circuit while maintaining synchronization and reliability at column 2, lines 6-15. In addition, Georgiou describes cooperatively modulating the clock frequency sufficiently to maintain system synchronization at the reduced supply voltage at column 4, lines 36-39 and at column 5, lines 8-12. Therefore, Georgiou discloses cooperatively adjusting the clock frequency in response to the temperature (power) signal such that system synchronization of the whole chip is maintained. It would have been obvious to one having ordinary skill in the art at the time the invention was made to control an operating frequency of the clock generator in response to communications from other clock zones, as suggested by Georgiou, in order to maintain synchronization and reliability of the whole chip, to allow for communication between clock zones (functional units) and to synchronize the processing of data in the plurality of clock zones.

Per claims 3, 11 and 17:

Georgiou does not explicitly describe that frequency adjustments require at least one clock cycle as claimed. However, one clock cycle is the smallest unit of time that a synchronous operation could be performed in a computer system and it would have been obvious to one having ordinary skill in the art at the time the invention was made that cooperative adjustments to the clock frequency would require at least the smallest unit of time for performing a synchronous operation.

(10) Response to Argument

Double Patenting

A) Appellant has previously stated that it would file a terminal disclaimer to overcome this rejection should the double patenting rejection apply to the claims as allowed.

The examiner maintains the obviousness double patenting rejection for the reasons described in the above rejection. The claims have not been amended since appellant's previous offer to file a terminal disclaimer. Appellant's offer to file a terminal disclaimer does not overcome the obviousness double patenting rejection.

Claim Rejections - 35 USC § 103

Appellant's cited case law and purported requirements to establish a prima facie case of obviousness are off base in view of the supreme courts decision in *KSR v. Teleflex*, 550 U.S. ___, 82 USPQ2d 1385 (2007). The Supreme Court ruled that *Graham v. John Deere* controls obvious inquiries not a rigid application of the teaching/suggestion/motivation test. Teaching/suggestion/motivation test as a litmus test for obviousness is inconsistent with the Graham framework. Rigid preventative rules that deny factfinders recourse to common sense are neither necessary under our case law nor consistent with it. Where there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. *KSR International Co. v. Teleflex Inc.*, 550 U.S. ____, 82 USPQ2d 1385 (2007).

B1) Georgiou does not teach or suggest at least one sensor that generates a power signal indicative of a power supply voltage within the clock zone.

Appellant's specification (paragraph 13, lines 1-2) and claims (claim 9) both disclose that the sensor can be a thermal sensor/detector. Appellant has disclosed and claimed that the sensor is a thermal sensor and then seems to argue that a thermal sensor cannot perform the recited function of generating a power signal indicative of a power supply voltage within the clock zone. Georgiou's temperature sensor (T1) generates a power signal (signal 125) indicative of a power supply voltage (on-chip voltage regulator 330, VDD 325) within the clock zone (zone 116-1) with figures 1 and 5b and at column 4, lines 18-42. Furthermore, the temperature sensor T1 provides a measure of the power dissipated by functional unit 1 (clock zone 1). The power dissipation of functional unit 1 (clock zone 1) is directly related to the power supply voltage (V, voltage swing) of functional unit 1 (clock zone 1) as disclosed by Georgiou at column 3, lines 31-40 and column 4, lines 44-46 and 59-61. Therefore, the power signal generated by the temperature sensor is indicative of a power supply voltage within the clock zone because of both its relationship to voltage regulator 330/VDD 325 and its relationship to the voltage swing factor (V) in the measured power dissipation.

B2) Georgiou does not describe each clock zone including a clock generator and a controller.

The examiner disagrees with applicant's contentions. Georgiou describes that each clock zone includes a clock generator and a controller for controlling the operating frequency of the clock generator. In the above rejection, the examiner pointed to a claimed clock zone as corresponding to a functional unit and its associated control circuitry in elements 130, 330 and 430 of figure 1. These control circuitry elements include clock selector 430 (clock generator) and temperature decoder 130 (controller). Georgiou describes that clock selector 430 and decoder 130 may be implemented on-chip and associated with each independently controllable functional unit and that each functional unit may be operating under a different voltage and frequency combination according to the thermal feedback from its associated thermal sensor at column 5, lines

1-8. Therefore, Georgiou describes that the controller (decoder 130) controls each clock generator (clock selector 430) of each zone (functional unit and associated circuitry) independently. Both the clock selector 430 (clock generator) and the temperature decoder 130 (controller) include circuitry associated with each one of the functional units. Each function unit and its associated control circuitry (clock selector 430, voltage regulators 330 and temperature decoder 130) in Georgiou correspond to the claimed clock zone because each one of Georgiou's zones includes an independently controllable clock frequency generator that is controlled by controller/decoder 130. Applicant has argued that their claimed invention is different from Georgiou because the claimed system is a distributed system while Georgiou describes a centralized system. The examiner disagrees with applicant's contention that the claims recite a distributed system. The claims are directed to a CPU that includes multiple clock zones. There is no indication in the claims as to whether the clock zones may overlap such that some of the circuitry may be shared between clock zones as described by Georgiou. The claims are not limited to non-overlapping clock zones such as a distributed system in which no circuitry is shared. Although Georgiou describes centralized/shared controller and clock generator components, each functional units zone includes an independently controllable clock frequency generator that is controlled by controller/decoder 130 based on each functional units individual temperature sensor. Therefore, Georgiou discloses the claimed clock zones.

B3) There is no motivation to modify Georgiou to include a controller responsive to frequency adjustment communications from other clock zones.

The examiner has acknowledged in the above rejection that Georgiou does not explicitly describe frequency adjustment communications from other clock zones. However, Georgiou describes that synchronization problems may occur when clock frequencies are varied to different portions of a chip and there is a need for controlling power dissipation of a synchronous circuit while maintaining synchronization and reliability at column 2, lines 6-15. In addition, Georgiou describes cooperatively modulating the clock frequency sufficiently to maintain system synchronization at the reduced supply voltage at column 4, lines 36-39 and at column 5, lines 8-12. Therefore, Georgiou discloses cooperatively adjusting the clock frequency (and voltage) in response to the temperature (power) signal such that system synchronization of the whole chip is maintained (column 5, lines 8-12). Georgiou describes that decoder 130 (controller) communicates voltage and frequency commands to each zone using an address associated with each functional unit and line 280 of figure 1 and at column 7, lines 37-49. Since decoder 130 is a centralized unit that includes circuitry shared by each clock zone and is responsible for controlling the voltage and frequency of each clock zone, it provides for communication between clock zones by controlling the voltage and frequency of each zone in a way that maintains system synchronization. It would have been obvious to one having ordinary skill in the art at the time the invention was made that the process of controlling synchronization problems that may occur when clock frequencies are varied to different portions of a chip could require communications between the clock zones in order to maintain synchronization and reliability of the system as a whole. Such communications could obviously include reporting any changes in a clock zones frequency to other clock zones in order to maintain synchronization. Where there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, 82 USPQ2d 1385 (2007). One of ordinary skill in the art at the time of the invention could have provided control settings in temperature decoder 130 (controller) that allow for synchronization between the clock zones based on frequency/voltage settings (communications) of other clock zones in order to increase the performance of the chip while lowering overall power consumption thereby considering known options/trade offs between processing performance and reduced power consumption as suggested by Georgiou at column 5, lines 8-15.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Dennis M. Butler/
Dennis M. Butler
Primary Examiner

Conferees:

/Lynne H Browne/
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SUPERVISORY PATENT EXAMINER
10/1/07